REMARKS/ARGUMENTS

In the Office action dated June 3, 2005, claims 1, 2, 8 – 11, 14, 16 – 19, and 21 were rejected and claims 3 – 7, 12 – 13, 15, and 20 were objected to. Applicants hereby request reconsideration of the application in view of the below-provided remarks.

I. Allowable Subject Matter

Applicants note with appreciation that claims 3 – 7, 12 – 13, 15, and 20 were deemed to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In view of the below-provided remarks, Applicants have not rewritten the claims at this time.

II. Claim Rejections Under 35 U.S.C. 102

Independent Claim 11

Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,466,096 to DeVito. Applicants assert that claim 11 is not anticipated by DeVito for the reasons set forth below.

Claim 11 is a system for controlling a voltage controlled oscillator (VCO) in a bang-bang phase-locked loop. The claim recites:

> "a step size controller configured to:
> provide a first VCO control signal to the VCO upon establishing frequency lock, said first VCO control signal causing the VCO frequency to change by a first step size; and
> provide a second VCO control signal to the VCO some time after the VCO frequency has changed in response to the first VCO control signal, said second VCO control signal causing the VCO frequency to change by a second step size,
> wherein the first step size is larger than the second step size."
> (emphasis added)

DeVito does not disclose a bang-bang type phase detector and therefore 'step sizes' are not relevant

Claim 11 is directed towards a system that utilizes a bang-bang phase-locked loop PLL (see preamble). As described in paragraph [003] of Applicants' specification, PLLs that utilize bang-bang phase detectors are often referred to as bang-bang PLLs. Bang-

bang phase detectors provide a binary (i.e., up or down) output that represents the phase of the VCO signal relative to the input signal (i.e., whether the phase of the VCO is early or late). The binary output is used to change the frequency of the VCO in discrete steps. The limitations of claim 11 are directed to the size of the frequency step that is caused by a bang-bang PLL (i.e., the first step size and the second step size). In contrast to claim 11, DeVito discloses a PLL that utilizes a linear or analog phase detector. Linear or analog phase detectors provide an output that is proportional to the phase difference between the VCO and the input signal. The VCO frequency is then changed in proportion to the phase difference. Because DeVito does not disclose a bang-bang type phase detector, which provides a binary output that causes the frequency of the VCO to change in discrete steps, there is no need for DeVito to describe the concept of a step size. Indeed, DeVito does not mention the concept of a "step size" related to the disclosed phase detector (20). Further, Applicants have found no mention of a step size controller that provides two different VCO control signals that cause the frequency of a VCO to change by two different step sizes as recited in claim 11. As a result, Applicants assert that claim 11 is not anticipated by DeVito.

DeVito does not disclose first and second VCO control signals that are provided "upon establishing frequency lock"

As recited in claim 11, the first VCO control signal is provided to the VCO "upon establishing frequency lock" and the second VCO control signal is provided to the VCO "some time after the VCO frequency has changed in response to the first VCO control signal." That is, both the first and second VCO control signals are provided to the VCO only after frequency lock has been established.

In the systems disclosed by Applicants and DeVito and as is well-known in the field, a frequency detector controls the VCO until the frequency of the VCO is within a "deadband region" or "target range" of the frequency detector. Once the frequency of the VCO is within the "deadband region" or "target range" of the frequency detector, the system is considered to be in "frequency lock" and control of the VCO is shifted over to the phase detector. This process is described in Applicants' specification at, for example, paragraphs [002] and [0027] and clearly depicted in Fig. 2. This process is described by DeVito at col. 3, lines 15 – 27, col. 5, lines 4 – 19, and the description related to Fig. 2. As described by DeVito, the frequency detector controls the VCO through its corresponding "coarse tune" signal when the frequency of the VCO is outside the target

range (i.e., when the system is out of lock) and the phase detector controls the VCO through its corresponding "fine tune" signal when the frequency of the VCO is within the target range (i.e., when the system is in frequency lock). In particular, with reference to the frequency detector (32) in Fig. 1, DeVito discloses:

> "if the frequency difference is within a prespecified target frequency range ("target range"), the frequency detector 32 delivers no output signal toward the upstream circuit elements (discussed below). If the frequency difference is outside of the target range, however, then a difference signal is delivered to the upstream circuit elements."

As disclosed by DeVito, the "coarse tune" signal from the frequency detector controls the frequency of the VCO until frequency lock is established, at which point, control of the VCO is left to the "fine tune" signal from the phase detector.

Claim 11 is rejected under the logic that the "coarse tune" and "fine tune" signals disclosed by DeVito anticipate the first and second VCO control signals and the corresponding first and second step sizes as recited in claim 11. Claim 11 recites a system in which the first and second VCO control signals are provided to the VCO "upon establishing frequency lock." That is, both the first and second VCO control signals are provided to the VCO only after frequency lock has been established. Further, the first and second VCO control signals cause the VCO frequency to change by first and second step sizes, respectively. In contrast, in the system of DeVito, the "fine tune" signal is the only signal provided to the VCO upon establishing frequency lock (i.e., once control of the VCO is shifted from the frequency detector to the phase detector). As outlined above, the "coarse tune" signal controls the VCO before frequency lock is established and the "fine tune" signal controls the VCO after frequency lock. DeVito does not disclose providing two VCO control signals to the VCO "upon establishing frequency lock" and DeVito does not disclose that the "fine tune" signal causes the VCO frequency to change by first and second step sizes. Further, because DeVito does not disclose a bang-bang type phase detector, the concept of step sizes is not relevant to DeVito. In sum, because DeVito does not disclose first and second VCO control signals that are provided to the VCO upon establishing frequency lock, Applicants assert that claim 11 is not anticipated by DeVito.

Dependent Claim 14

Claim 14 recites "wherein the step size controller is configured to transition to providing the second VCO control signal in response to a control signal that indicates frequency lock." Claim 14 is rejected under the logic that "the output of phase detector 20 is seen as a control signal to indicate frequency lock and to provide the second VCO control signal." (Office action, page 2) Applicants assert that the output of the phase detector of DeVito is not a control signal that indicates frequency lock because the output of the phase detector, identified as the "fine tune" signal, is provided to the VCO whether or not the system is in frequency lock, see DeVito col. 4, lines 8 – 24. Further, the "fine tune" signal of DeVito has no control over whether or not the "coarse tune" signal is generated. As described above, the "coarse tune" signal is generated when the frequency of the VCO is outside the target range of the frequency detector. Because the output of the phase detector of DeVito is not a control signal to indicate frequency lock, claim 14 is not anticipated by DeVito.

Claim 1

Claim 1 is a method claim that has limitations similar to the system of claim 11. Because of the similarities between claims 1 and 11, Applicants assert that the remarks provided above with respect to claim 11 apply also to claim 1.

Dependent Claim 8

Claim 8 is a method claim that has limitations similar to the system of claim 14. Because of the similarities between claims 8 and 14, Applicants assert that the remarks provided above with respect to claim 14 apply also to claim 8.

Dependent Claims 2, 9, and 10

Applicants assert that claims 2, 9, and 10 are allowable based on an allowable base claim.

Independent Claim 16

Claim 16 is a system claim that has limitations similar to the system of claims 11 and 14. In particular, claim 16 includes "timing control logic configured to control the timing of changes in VCO frequency step size in response to a control signal that indicates frequency lock." Because of the similarities between claims 16 and claims 11

and 14, Applicants assert that the remarks provided above with respect to claims 11 and 14 apply also to claim 16.

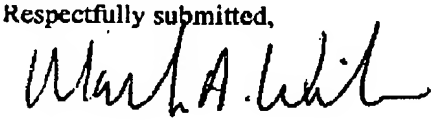
Dependent claims 17 – 19 and 21

Claim 17 recites "delay logic" for "delaying the control signal that indicates frequency lock." Applicants assert that DeVito does not disclose a control signal that indicates frequency lock as stated above with reference to claim 14. Because DeVito does not disclose a control signal that indicates frequency lock, DeVito has no need to disclose delay logic for delaying the non-existent control signal.

Claims 18, 19, and 21 relate to details of the step size logic. As stated above, DeVito does not disclose a binary phase detector and therefore does not disclose the concept of a step size. Because DeVito does not disclose the concept of a "step size" there is no need to disclose step size logic or the details of step size logic as recited in claims 18, 19, and 21.

Applicants respectfully request reconsideration of the claims in view of the remarks made herein.

Respectfully submitted,



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